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Benchmarking organic thin film transistor inverter design styles

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ABSTRACT

Organic thin-film transistors (OTFTs) are a promising technology for large-area electronics; choosing an appropriate circuit style is critical to enhancing OTFT circuit functionality and reliability. Here, we design and evaluate different types of static and dynamic logic based on complementary and p-type only technology styles, benchmarking their performance under equivalent processing and testing conditions. We find that differences in off characteristics between n-type and p-type OTFTs to be the primary factor for the choice of logic style. For complementary technology, we conclude that static logic is preferred over dynamic logic considering limited n-type transistor off characteristics, integration density, and delay. In the case of p-type transistors, pre-discharge dynamic logic is preferred over static logic, primarily due to the static power efficiency from good p-type transistor off characteristics. We expect this evaluation to be helpful for assisting design style decisions as these technologies continue to mature and develop.

1. Introduction

Organic electronics have realized considerable advances in the past few decades. The compatibility of organic semiconductors with low-temperature and solution processing makes them an important technological option for flexible and large-area applications. In addition to material and device-level research, an increasing number of complex applications have been developed based on organic thin film transistors (OTFTs), such as radio frequency identification, or RFID, tags [1–4], large-area sensor arrays [5–8], analog-to-digital converters [9], digital-to-analog converters [10], and microprocessors [11]. These demonstrations and their potential application make organic circuits a compelling alternative technology.

Unlike in Si circuits where complementary, or CMOS, logic is the mainstream circuit style, the choice of logic style for organic semiconductors is more variable. Compared to complementary logic, p-type only monotype logic has been employed in previous benchmarking work [12,13]. There are several reasons for this: first, p-channel organic semiconductors were among the first adopted materials, and early on in the study of organic transistors, they significantly outperformed n-channel logic in terms of both carrier mobility and device stability. Thus, the large imbalance of hole and electron mobilities in a complementary circuit makes p-type only logic favorable. Second, the processing compatibility for complementary logic is challenging. Usually for organic semiconductors, the optimized condition of interface, processing temperature, and metal contacts are variant for n-type and p-type semiconductors, making it challenging to integrate both materials with optimized performance. As a result, p-type only logic, such as zero-V_{GS} logic and pseudo-CMOS logic, has been widely implemented in different applications [11,5,14].

However, mono-type logic has intrinsic drawbacks regarding power consumption, integration density, and speed. With recent developments of n-type semiconductors with higher mobility and stability [15–18,19], more moderate processing techniques, and advancements in patterning protocols [20–22], there is an increasing number of applications based on complementary logic [23,24,1]. Therefore, the question remains as to whether mono-type logic is the best choice for organic circuits. In an effort to answer this question, this work conducts an objective benchmarking of various logic styles to inform circuit optimization and application viability, and seeks to draw generally applicable conclusions. To the best of our knowledge, this is the first work that provides a comprehensive benchmarking (including complementary, p-type only, static, and dynamic) for organic thin film transistor circuit styles.

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2. Fabrication, characterization, and modeling

To construct a practical framework to benchmark different logic styles, we first introduce the design and fabrication of OTFTs as the fundamental building block.

2.1. Fabrication

The OTFTs in this work are based on bottom gate, top contact devices, with layout and schematic view of the OTFT sample illustrated in Fig. 1 with additional information regarding circuit transistor and pin count and area presented in Table 1. Starting from a 3 × 3 cm Eagle XG glass substrate, a 50 nm gate electrode (Cr for p-type, Ti for n-type) is e-beam evaporated at a rate of 1 Å/s, wet etched by Cr-7 etchant (for Cr) and H_2O_2:HF:H_2O = 1:1:30 solution (for Ti). Then a layer of 120 nm Al_2O_3 is deposited via 1000 cycles of atomic layer deposition (ALD) at 300 °C, wet etched by 85% H_3PO_4 solution. Then the sample is immersed in 10 mM octadecyltrichlorosilane (OTS) solution for 4 h to form a self-assembled monolayer (SAM), followed by thermal evaporation of 50 nm of C_{60} (for n-type) and pentacene (for p-type) in a vacuum chamber with a base pressure of 1 × 10^{-7} Torr. Finally, Al (for n-type) and Au (for p-type) are separately deposited via thermal evaporation to form source/drain electrodes. In this way, both the active and source/drain layers are patterned via shadow mask.

2.2. Transistor characterization

The device characterization is measured using a probe station in a nitrogen-filled glove box. A HP4155A parametric analyzer is used for DC measurement, while a RIGOL DS1054Z Digital Oscilloscope is used for AC measurement.

The drain current-gate-source voltage (I_D-V_{GS}) transfer characteristics of pentacene and C_{60} OTFTs are shown in Fig. 2, and the extracted parameters are listed in Table 2. The transistors exhibit good yield and uniformity with linear mobility, μ = 0.20 $cm^2V^{-1}s^{-1}$, and subthreshold slope of 190 mV/dec for a representative p-type transistor, and μ = 0.22 $cm^2V^{-1}s^{-1}$ with subthreshold slope of 200 mV/dec for a representative n-type transistor, both at a drain-source voltage of V_{DS} = 1 V. As is clear from the transfer curves, both n-type and p-type transistors are working under enhancement mode with a close-to-zero threshold voltage (V_T), which can be expected to allow for low-voltage and power-saving operation of OTFT circuits. In addition, the nearly matching mobilities of n-type and p-type transistors can be expected to benefit the performance of complementary logic design. Information regarding contact resistance is summarized in Section 1 of the supporting information, with a transmission line measurement shown in Fig. S1, and contact resistance values presented in Table S1. The n-type transistor is shown to have higher contact resistance than the p-type transistor.

The major difference between the n-type and p-type OTFTs is their off characteristics, and the n-type OTFT has an order of magnitude higher drain leakage current than the p-type OTFT. The high leakage current could lead to higher static power consumption in static logic and a shorter evaluation time window in pre-charge dynamic logic for n-type OTFTs.

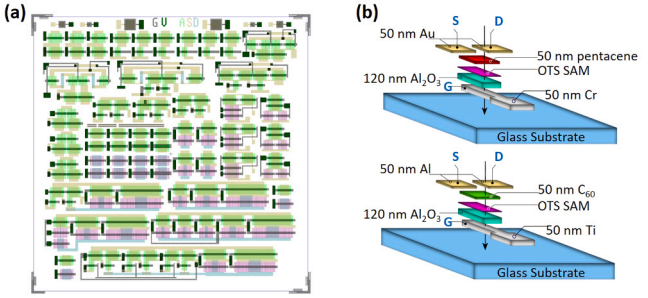

Fig. 1. (a) Layout of an OTFT sample over a 3 × 3 cm substrate. (b) Schematic view of pentacene and C_{60} OTFTs.

Table 1
Layout information for OTFT and circuit designs.

Unit Name	Transistor Count	Pin Count	Area (mm^2)
Individual transistor	1	3	2.8
Complementary inverter	2	4	7.1
Diode-load inverter	2	4	7.1
Biased-load inverter	2	5	7.1
Pseudo-D inverter	4	5	11.8
Pseduo-E inverter	4	5	10.6
Complementary ring oscillator	6	3	27.5
Pseudo-E ring oscillator	12	4	46.5
Complementary pre-charge inverter	3	5	9.7
Complementary pre-discharge inverter	3	5	9.7
P-type pre-discharge inverter	3	6	9.7

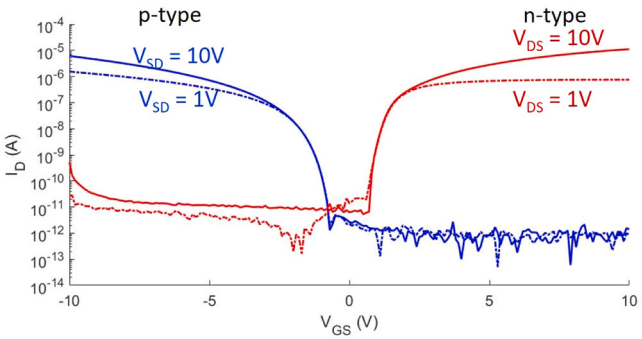

Fig. 2. I_D−V_{GS} transfer characteristics of p-type and n-type transistors at $|V_{DS}|$ = 1 V and $|V_{DS}|$ = 10 V, channel length L = 40 μm, channel width W = 1000 μm.

To better design and optimize OTFT circuits, a level 61 TFT model developed by Rensselaer Polytechnic Institute (RPI) [25] is used to simulate the circuit behavior. The RPI model is designed for 3 terminal TFTs working under accumulation mode and with a sufficient number of parameters to describe V_T, sub-V_T regime, leakage current, and carrier mobility. Fig. 3 plots the simulated data against the measured experimental data. In general, the simulated data show good consistency with the experimental data, especially in the transient region. Given this, we use the model in our subsequent work to inform transistor sizing within the circuit design.

3. Benchmarking of Static Inverters

In this section, we compare the merits and disadvantages of various designs for static inverters.

3.1. Inverter designs compared

To start, we compare static inverter characteristics based on complementary and p-type only logic. The schematics and layouts of five different designs are shown in Fig. 4, including complementary (Fig. 4(a)), diode-load (Fig. 4(b)), biased-load (Fig. 4(c)), pseudo-D (Fig. 4(d)), and pseudo-E (Fig. 4(e)) designs. The simplest design is complementary logic with balanced pull-up and pull-down networks. For p-type only logic, the load transistor is replaced by a p-type transistor with inherently weaker pull-down strength, which as a consequence has a negative impact on performance. For two-transistor based designs, the two most common structures are zero-V_{GS} load and diode-load, both of which are

Table 2
Extracted parameters of p-type and n-type transistors at $|V_{DS}| = 1$ V and $|V_{DS}| = 10$ V (SS: subthreshold slope, I_{on}: on-state drain current at $|V_{GS}| = 10$ V), I_{off}: off-state drain current at $|V_{GS}| = 5$ V).

Name	p-type, V_{SD}= 1 V	p-type, V_{SD}= 10 V	n-type, V_{DS}= 1 V	n-type, V_{DS}= 10 V
μ_{linear} ($cm^2\ V^{-1}\ s^{-1}$)	0.20	0.12	0.22	0.12
V_T (V)	−1.2	−1.3	0.8	0.7
SS (mV/dec)	190	180	200	150
I_{on} (μA)	1.6	6.3	0.75	11.1
I_{off} (pA)	0.8	0.9	5.0	11.3
I_{on}/I_{off}	2.0×10^6	7.0×10^6	1.5×10^5	9.8×10^5

ratioed with a load transistor for the pull-down network. For the zero-V_{GS} load inverter, the gate and source of the load transistor are shorted, therefore requiring the load transistor to operate in depletion mode ($V_T > 0$) for fast switching of the pull-down network. The implementation of a zero-V_{GS} load inverter is typically combined with a dual-V_T design with depletion load transistor [26], thus it is not favorable for single V_T enhancement mode ($V_T < 0$) transistors in this work. For diode-load inverters, the gate and drain of the load transistor are shorted to ground. While such inverters can operate normally for enhancement mode p-type transistors, it relies on a large size ratio between drive and load resistor for adequate voltage swing, creating a tradeoff that causes these inverters to suffer from low noise margin and gain.

To further improve the p-type only inverter performance, one common method is to add a third power rail, V_{SS}, to enhance the pull-down strength [27]. The impact of V_{SS} on inverter performance is shown in Fig. 5. The biased-load inverter directly adds V_{SS} on the load transistor, which gives the circuit stronger pull-down strength. However, with increasing V_{SS}, it is difficult to maintain a high output since the drive transistor will compete with the low-resistance load transistor when V_{IN}=0. From Fig. 5(a), it is evident that a trade-off exists between a balanced transfer curve and gain. To provide more details of two-transistor-based p-type only inverters, Fig. S2 in the supporting information shows the impact of transistor sizing for diode-load and biased-load inverters. Compared to the biased-load design, pseudo-D and pseudo-E logic add a level-shifter stage such that the gate bias on the load transistor of the second stage indirectly depends on V_{SS}. This enables V_{SS} to control the switching threshold with an enhanced voltage swing from 0 to V_{DD}, providing the potential for better performance than two-transistor-based inverter designs. For the pseudo-D inverter design, since the first stage is still a zero-V_{GS} load inverter, it has the same problem of a weak pull-down strength from the gate-source shorted enhancement load-transistor. From Fig. 5(b), it can be seen that V_{SS} has very weak control over the switching threshold, resulting in a poor noise margin. Although the pseudo-D inverter has high static voltage gain from the zero-V_{GS} design [28], we expect the transient speed will be slow, due to the high resistance/low output current of the level-shifter stage. In comparison, for the pseudo-E inverter (Fig. 5(c)), the voltage transfer curve can shift over a wide range with increasing V_{SS}, and provides for a high noise margin that is optimized at $V_{SS} = -11.5$ V. Also, the pseudo-E inverter operates at a relatively fast speed, as shown in Fig. 5(d), with a transient response that is optimized at $V_{SS} = -20$ V.

The transfer and transient characteristics of the five circuit designs at $V_{DD} = 10$ V are shown in Fig. 6, with the extracted parameters from these circuits provided in Table 3. The transfer and transient characteristics of the five circuit designs at $V_{DS} = 1$ V is shown in Fig. S3 in the supporting information. The complementary logic circuit shows the best performance with high DC voltage gain, high noise margin, and fast switching speed due to its balanced pull-up/pull-down network and simple structure. The NAND based on complementary logic is also characterized in Fig. S4, with parameters extracted in Table S2 in the supporting

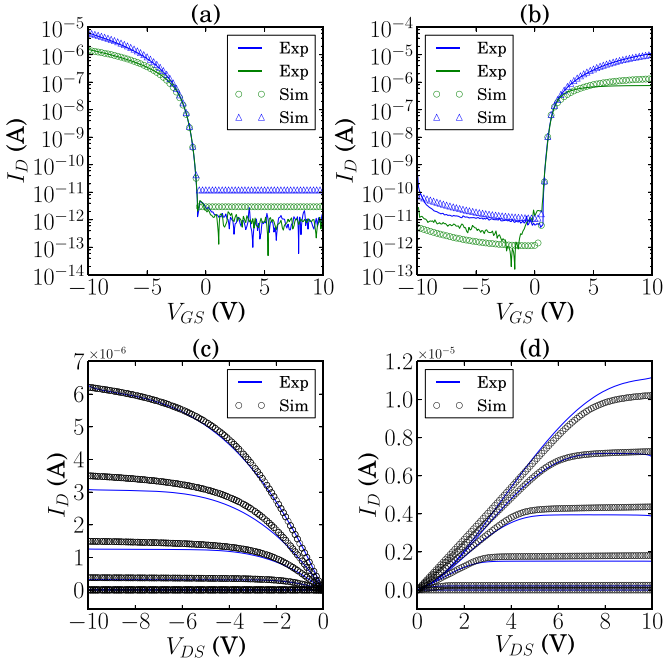

Fig. 3. Comparison of measured and modeled transfer and output characteristics of pentacene (a, c) and C_{60} (b, d) OTFTs.

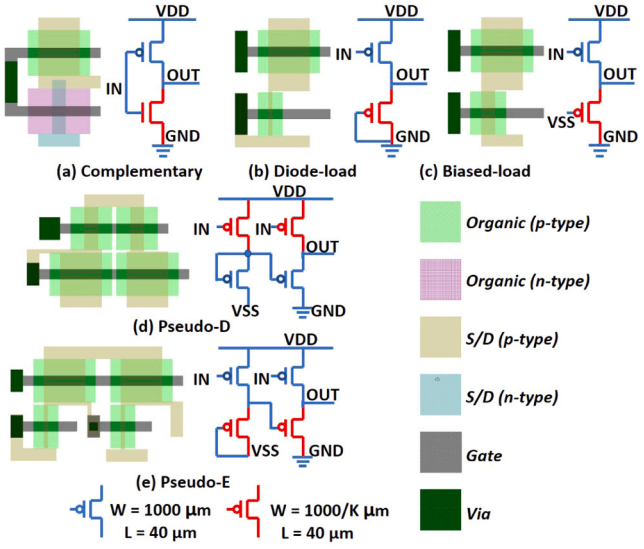

Fig. 4. Schematics and layouts of OTFT based static inverters, including (a) complementary, (b) diode-load, (c) biased-load, (d) pseudo-D, and (e) pseudo-E. The channel lengths are 40 µm, the maximum channel width is 1000 µm for transistors in blue, size ratio parameter K is defined as the transistor in red with 1000/K µm channel width.

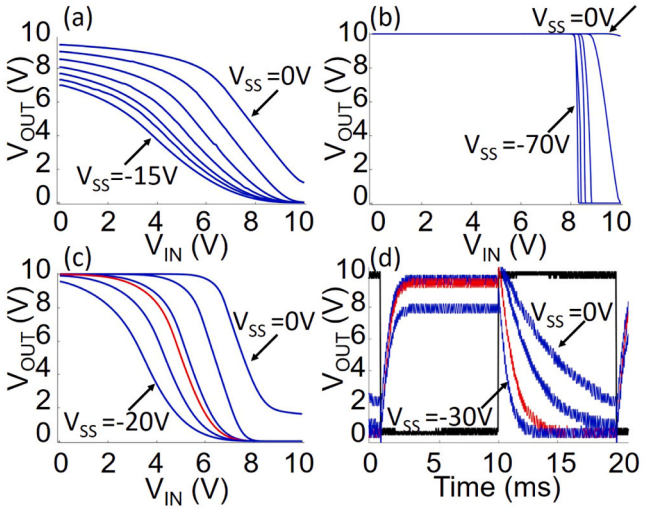

Fig. 5. The impact of V_{SS} on the transfer characteristics of (a) biased-load inverter, V_{SS} varies from 0 to − 15 V in − 2.5 V steps, (b) pseudo-D inverter, V_{SS} varies from 0 to − 70 V in − 10 V steps, (c) pseudo-E inverter, V_{SS} varies from 0 to − 20 V in − 5 V steps. The transfer curve is optimized at V_{SS} = −11.5 V in red curve. (d) The impact of V_{SS} on the transient characteristics of a pseudo-E inverter. The transient response is optimized at V_{SS} = −20 V in red curve.

information. For p-type only logic, from the previous discussion, we expect the additional level-shifting stage and the V_{SS} terminal will improve the performance, and the measured results are in line with expectations. The pseudo-E inverter is the best choice for single-V_T, enhancement mode p-type only logic, with high switching threshold tunability, fast transient response, and moderate voltage gain.

3.2. Comparison of complementary and pseudo-E inverters

Since, in our benchmarking, pseudo-E logic emerged as the optimal p-type only logic design, in this section we compare its performance with complementary logic in terms of sizing and power consumption.

3.2.1. Impact from transistor sizing

Fig. 7 shows the performance of pseudo-E and complementary inverters with different sizing. For complementary logic, the n-type transistors exhibit stronger drive strength than p-type ones, resulting in an optimized design with wider pull-up p-type devices. The size is optimized at K = 3, with a $V_{DD}/2$ switching threshold, and maximum noise margin and voltage gain. The optimized sizing is in a narrow range since the noise margin and switching threshold primarily depend on the size ratio K. If transistors have a large variation of mobility and threshold voltage, it is challenging for complementary designs to work reliably.

In comparison, the pseudo-E design is less sensitive to the size

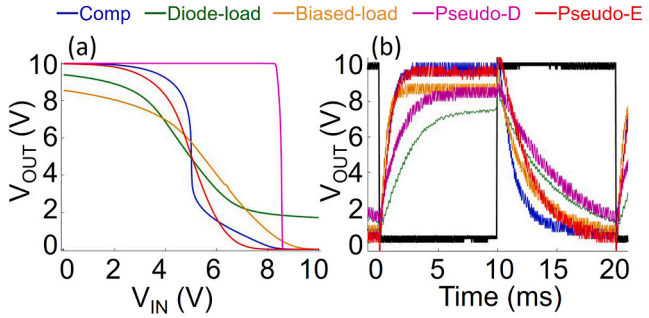

Fig. 6. (a) Transfer and (b) transient characteristics of various OTFT-based static inverters (Comp: Complementary).

Table 3
Extracted parameters of OTFT-based static inverters (NMH: noise margin high, NML: noise margin low).

Inverter Type	Comple-mentary	Diode-load	Biased-load	Pseudo-D	Pseudo-E
Gain	72	2.0	1.8	136	4.4
V_M (V)	5.0	5.0	5.3	8.4	5.0
V_{SS} (V)	N/A	N/A	−5.0	−70	−11.5
NMH (V)	3.0	1.2	0.5	1.4	2.5
NML (V)	2.7	1.0	0.8	8.2	2.8
Rise time (ms)	1.0	3.8	0.8	2.3	1.4
Fall time (ms)	2.2	5.3	5.6	5.1	4.9
Area (mm^2)	7.1	7.1	7.1	10.6	11.8

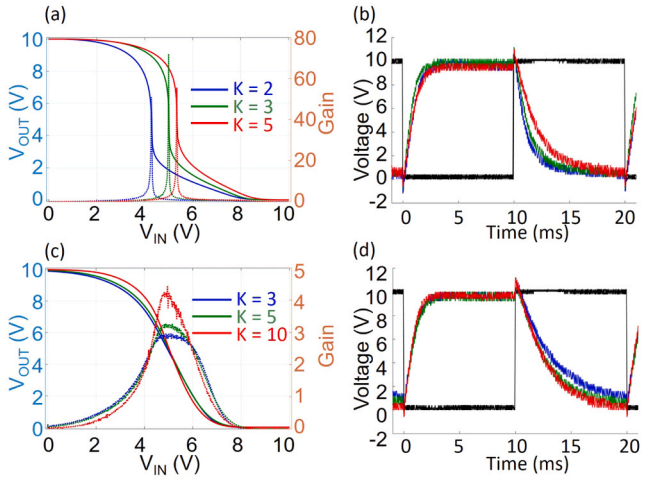

Fig. 7. The impact of transistor sizing on inverter performance. (a) Transfer characteristics and (b) transient characteristics of complementary inverter, the channel width W_{PU} = 1000 μm and W_{PD}= 500 μm, 330 μm, and 200 μm , corresponding to K = 2, 3, and 5. (c) Transfer characteristics and (d) transient characteristics of pseudo-E inverters, the channel length W_{PU} = 1000 μm and W_{PD} = 330 μm, 200 μm, and 100 μm, corresponding to K = 3, 5, and 10 (W_{PU}: channel width of pull-up transistor, W_{PD}: channel width of pull-down transistor, size ratio K = W_{PU}/W_{PD}).

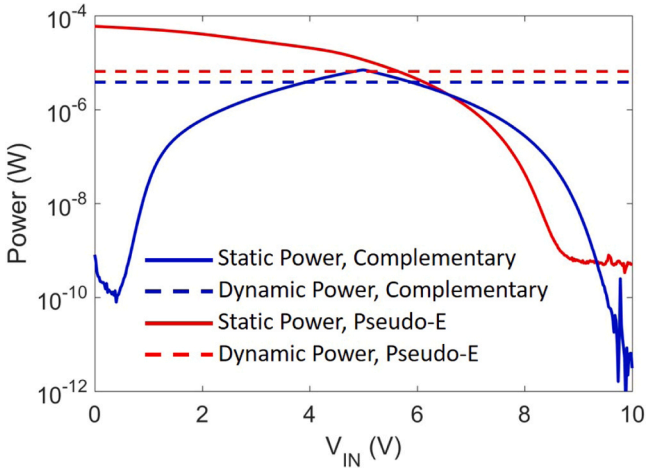

Fig. 8. Static power dissipation (solid lines) and dynamic power dissipation (dashed lines) for complementary/pseudo-E inverters as a function of V_{IN}. The dynamic power is estimated from $CV_{DD}^2 f$ with f = 50 Hz.

Table 4
Extracted power consumption parameters for complementary and pseudo-E inverters.

Inverter Type	Complementary	Pseudo-E
Static power low (W)	1.1×10^{-10}	7.2×10^{-5}
Static power high (W)	1.0×10^{-11}	6.8×10^{-10}
Static power max (W)	7.0×10^{-6} ($V_{IN} = 5$ V)	7.2×10^{-5} ($V_{IN} = 0$ V)
Estimated dynamic power (W)	3.8×10^{-7}	6.5×10^{-7}

parameter as the switching threshold can be tuned post-fabrication through V_{SS}. Over a wide size range, the inverters can operate optimally via tuning of V_{SS}. The gain and noise margin slightly increase with increasing size ratio K. However, as K cannot be excessively large due to increased power consumption, V_{SS} voltage, and area, we choose K = 10 as an appropriate size ratio a balance of performance, area, and power consumption.

3.2.2. Power consumption analysis

Fig. 8 shows the static and dynamic power consumption for pseudo-E and complementary inverters, with the power consumption parameters summarized in Table 4. The dynamic power is estimated from $C \times V_{DD}^2 \times f$ where the input transition frequency $f = 50$ Hz. The complementary inverter consumes very low static power when the input is at $V_{IN} = 0$ or $V_{IN} = V_{DD}$. The lowest power consumption is at $V_{IN} = V_{DD}$. This results from the fact that the p-type transistor has better off-state characteristics than the n-type transistor. The highest power consumption case (when $V_{IN} = V_{DD}/2$) is rare under normal circuit function. As a result, the dynamic power consumption dominates since it is more than 3 orders of magnitude higher than stable input static power. By contrast, for pseudo-E logic, the static power increases monotonically with decreasing V_{IN}. When the input is low, the drive transistor is on, the load transistor is not completely turned off, resulting in large static current. The pseudo-E inverter consumes 70% more static power, 10 times more than complementary logic. Most importantly, in the worst case ($V_{IN} = 0$), the pseudo-E inverter consumes 70,000 times more static power than complementary logic, with the static power accounting for more than 99% of overall power consumption.

3.2.3. Ring oscillator

To further compare the functionality of the complementary and pseudo-E logic, we investigated the performance of ring-oscillators. Fig. 9(a) shows the structure of 3-stage ring-oscillators with an output buffer, implemented for both complementary and pseudo-E inverter. From Fig. 9(b,c), we see the complementary circuit begins to oscillate at $V_{DD} = 3$ V with a frequency of 10.4 Hz, whereas the pseudo-E circuit starts to oscillate at $V_{DD} = 4$ V with a frequency of 14 Hz. At $V_{DD} = 10$ V, the complementary circuit operates 2.3 times faster than the pseudo-E design. For pseudo-E logic, as Fig. 9(d) illustrates, there is a trade-off between the operating speed and amplitude/noise margin of pseudo-E ring-oscillators. Since the delay from the pull-down network dominates, when negative V_{SS} increases, the pull-down delay is reduced, resulting in operation at increasing frequency. The trade-off is that the stronger biased V_{SS} also reduces the noise margin. For $V_{DD} = 5$ V, the pseudo-E ring-oscillator starts to oscillate at $V_{SS} = -4$ V, and ceases to oscillate at $V_{SS} = -10$ V. In summary, due to the higher gain, noise margin, and lower stage delay, the complementary ring-oscillator runs about 2.3 times faster, with 50% of the transistor counts and 60% of the area when compared to pseudo-E ring-oscillators.

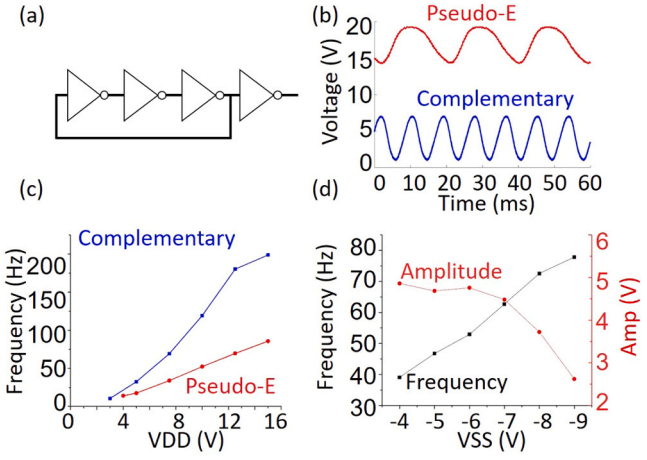

Fig. 9. (a) Schematic of a 3-stage ring oscillator with buffer. (b) Ring oscillator curve from complementary and pseudo-E logic at $V_{DD} = 10$ V. For pseudo-E logic, $V_{SS} = -11.5$ V. (c) Comparison of oscillation frequency as a function of V_{DD} for complementary and pseudo-E logic. (d) Comparison of oscillation frequency and amplitude at different V_{SS} for pseudo-E logic.

4. Benchmarking of dynamic inverters

The circuit designs presented earlier are all based on static logic, and thus the output depends only on the input signal. In this section, we benchmark inverters based on dynamic logic. The operation of dynamic logic circuits is divided into two phases, pre-discharge for p-type evaluation logic (or pre-charge for n-type evaluation logic) and evaluation. Taking the pre-discharge dynamic inverter as an example, when CLK = 1, the dynamic logic operates in the pre-discharge phase, while the inverter output is pre-discharged to 0. When CLK transitions to 0, the inverter enters the evaluation phase and the output signal is evaluated to be the inverse of the input signal. The pull-up and pull-down networks for dynamic logic are clocked to operate at different phases and will not conduct at the same time. As such, dynamic logic is expected to benefit from faster switching speed, lower static power dissipation, and reduced transistor count when the number of logical inputs to a gate is high.

Three different types of dynamic inverters are discussed in this work, complementary pre-charge, complementary pre-discharge, and p-type

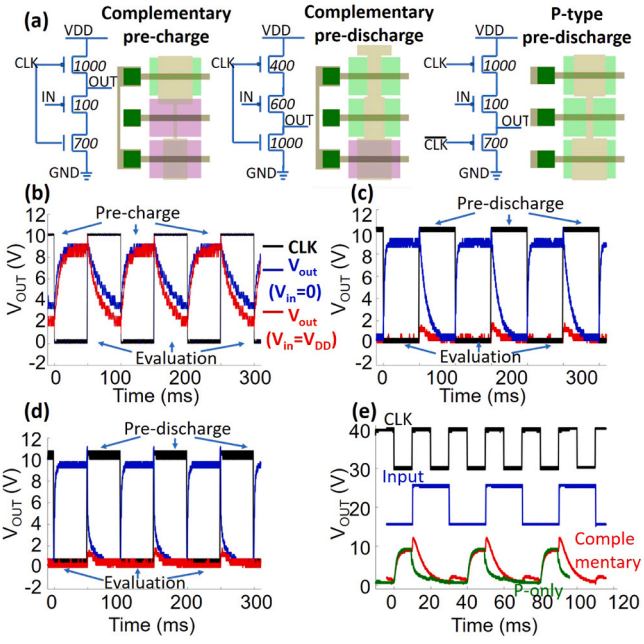

Fig. 10. (a) Schematics and layouts of three different dynamic logic designs, left: complementary pre-charge, center: complementary pre-discharge, right: p-type only pre-discharge. Transient characteristics from static input of (b) complementary pre-charge, (c) complementary pre-discharge, and (d) p-type only pre-discharge logic. (e) Transient characteristics from dynamic input of pre-discharge inverters.

Table 5
Extracted parameters for dynamic inverters. The dynamic power is estimated at a clock frequency of $f = 50$ Hz, assuming the worst case situation (input set as low for pre-discharge, high for pre-charge), such that the output node toggles at the same frequency as the clock.

Dynamic Inv Type	Complementary precharge	Complementary predischarge	P-type predischarge
Functional	N	Y	Y
Total channel *W* (mm)	1.8	2.0	1.8
Estimated dynamic power (W)	5.3×10^{-7}	5.9×10^{-7}	5.3×10^{-7}
Logic swing high (V)	6.7	8.6	9.0
Logic swing low (V)	6.2	1.0	1.0
Rise time (ms)	11	4.5	4.5
Fall time (ms)	39.5	23.5	15.5
Rise delay (ms)	5.0	1.5	0.8
Fall delay (ms)	9.5	8.0	1.5

only pre-discharge logic. For the p-type only design, complementary CLK and CLKN signals are required. The schematics and layouts of the dynamic inverters are shown in Fig. 10(a), with extracted parameters summarized in Table 5.

In CMOS logic, pre-charge logic is widely used due to the better performance of the n-type transistor. However, in this work, the pre-charge device showed poor performance, as shown in Fig. 10(b). At low input state, the output node failed to hold the pre-charge state and the voltage fell to a low state. As a result, it is difficult to differentiate the output state between low input (blue curve, with 6.2 V logic swing) and high input (red curve, with 6.7 V logic swing). The problem likely comes from the fact that the n-type C_{60} transistor has higher drain-source leakage current (an order of magnitude higher than the p-type transistor). This leakage path from the pull-down network can therefore discharge the capacitor of the output node. To address this problem, a pre-discharge design is preferred since, in the worst case, the high voltage from the output only needs to hold for half of the CLK cycle in contrast to the pre-charge design's full CLK cycle.

In the case of pre-discharge dynamic logic (see Fig. 10(c,d)), both the complementary and p-type-only designs can function properly at low frequency. The p-type-only design has better pull-down performance. From Fig. 10(e), at CLK = 50 Hz, the complementary pre-discharge operates with poor gain, long fall time, and long delay, whereas the p-type only pre-discharge device can still operate properly. The transient response indicates that for pentacene/C_{60} OTFT circuits, p-type transistors operate better for dynamic logic design.

From the above analysis, for complementary logic design, the benefits of dynamic logic design are limited, mainly owing to the high leakage from the n-type transistor. By contrast, dynamic logic is preferred for p-type only design. The p-type only dynamic inverter has comparable operating speed to pseudo-E static logic, consumes 17% less area, and has a 25% lower transistor count. Unlike Si-based dynamic logic, which suffers from high dynamic energy dissipation, for OTFT based p-type only logic, the static power consumption is comparable to the dynamic power consumption. The dynamic logic has this advantage due to its close-to-zero static power consumption. In the extreme case ($V_{IN} = 0$ V), for p-type only static logic, the static maximum power consumption is 7.2×10^{-5} W, while for the dynamic logic, the overall power consumption is 5.3×10^{-7} W, two orders of magnitude lower.

If one only considers performance from the single-stage inverter, the dynamic logic outperforms. But we should still consider extra cost from dynamic logic. First, the extra CLK (and CLKN for p-type only discharge) signal is required, and in practice, phase fluctuations and frequency drift from the non-ideal clock will result in deteriorated performance. Moreover, to avoid a charge sharing problem, static logic is still required (like in domino logic) to cascade between different stages. The benefits in terms of area, transistor count, and power consumption are largely offset when we consider large-scale system design.

Table 6
Summary of benchmarking for static and dynamic logic based on complementary or p-type only transistors.

	Static logic	Dynamic logic
Complementary	Preferred design • High voltage gain • High integration density • Low static power	Non-preferred design • High n-type leakage current • Pre-charge: nonfunctional • Pre-discharge: long pull-down delay
P-type only	Non-preferred design • High static power • Low voltage gain • Low integration density	Preferred design • Low static power • Short pull-down delay • Simpler fabrication process

5. Conclusions

In this work, we performed a novel and objective benchmarking of static and dynamic circuit designs using p-type only and complementary OTFTs. The off characteristics difference is the primary factor for the choice of logic style due to the significant impact on dynamic logic functionality and static power consumption. As summarized in Table 6, for complementary logic, static logic is preferred as complementary dynamic logic suffers from high n-type transistor leakage current. For p-type only logic, dynamic logic is preferred due to better off characteristics from the p-type transistors and lower static power consumption.

Overall, we expect that complementary static logic should be implemented for large-scale system design, assuming that n-type OTFTs can be made to be as stable as p-type devices. P-type only pre-discharge dynamic logic can be an alternative technology for applications concerned with area and power consumption and warrants further development. P-type only pseudo-E static logic can also be an alternative technology with better post-fabrication tunability and a simpler fabrication process flow.

CRediT authorship contribution statement

Zhuozhi Yao: Conceptualization, Methodology, Writing - original draft preparation. **Ting-Jung Chang:** Visualization, Simulation, Software. **David Wentzlaff:** Writing - reviewing & editing. **Barry Rand:** Writing - review & editing, Validation, Supervision.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Appendix A. Supporting information

Supplementary data associated with this article can be found in the online version at doi:10.1016/j.synthmet.2021.116825.

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